

# A 5.8ppm/°C Bandgap Reference with a Preregulator

Feiyan Mu<sup>1</sup>, Mingying Du<sup>1</sup>, Jie Lin<sup>2</sup>

1. Department of Electronic Engineering, Chengdu College of UESTC

2. Long Xin Co. Ltd. Chengdu China

mufeiyan@163.com

**Abstract**—To reduce the temperature draft of accurate analog to digital converters, a voltage reference introduced in 0.5μm BiCMOS technology in this paper. With curvature compensation, a low offset operational amplifier and a temperature-compensated preregulator, the temperature coefficient of the reference is reduced to 5.8ppm/°C and the operating temperature range is extended to between -55°C and +125°C. Moreover, the reference's PSRR at DC is 92dB, revealing a good power supply rejection of the circuit.

**Keywords**—bandgap reference; curvature compensation; low offset; preregulator; BiCMOS

## I. INTRODUCTION

Bandgap references are essential building blocks in many analog and mixed-signal circuits. Recently, precision circuitries such as data converters with resolutions of more than 20 bits are emerged, which higher the requirements of the references they used [1] [2]. Also, the operating temperature range is considered to be more important than before—the reference should work well over the industrial temperature range of -40°C to +125°C. Further more, in order to eliminate the influence of noise coupled from, the reference should not be sensitive to the power supply [2]. Finally, in consideration of battery life span, the circuit should consume as less power as possible. However, the conventional references, due to the nature of first order temperature compensation, have temperature coefficients over 20ppm/°C and operation temperature ranges of less than 100°C (-20°C~80°C) [3]-[5]. Moreover, considering that the control loop has very limited gain, power supply rejection ratio (PSRR) in conventional references hinders the whole system's performance.

A reference with a temperature coefficient of 5.8ppm/°C in an operation temperature range of -55°C~125°C is introduced in this paper. High PSRR is achieved to tolerate the power supply variations. The reference incorporates curvature compensation to eliminate the high order temperature dependences of bipolar devices. Also, the reference use an operational amplifier with low input offset to reduce the influence of nonidealities of circuit. A preregulator is designed to regulate the input node of the reference and PSRR of the reference are greatly improved without affecting the temperature performance.

## II. PRINCIPLES AND DESIGN CHALLENGES OF BANDGAP REFERENCE

### A. Principles of bandgap reference

The basic principle of a bandgap reference is to compensate the negative temperature coefficient of V<sub>BE</sub> of bipolar junction transistor (BJT) with a positive temperature coefficient voltage, for instance, the thermal voltage V<sub>T</sub>.

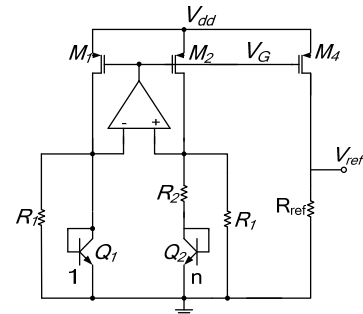


Fig. 1 A conventional reference.

A conventional current mode reference circuit implementation is shown in fig.1. The output of the reference can be written as:

$$V_{ref} = \left( \frac{V_T \ln n}{R_2} + \frac{V_{BE}}{R_1} \right) \cdot R_{ref} = \frac{R_{ref}}{R_1} \left( \frac{R_1}{R_2} V_T \ln n + V_{BE} \right) \quad (1)$$

where  $n$  is the emitter area ratio of transistor  $Q_1$  to  $Q_2$ . If the resistor ratio is carefully set, the first term in equation (1), which has a positive temperature coefficient, can compensate the negative temperature coefficient of  $V_{BE}$ . On top of that, the output voltage can be scaled by resistor ratio  $R_{ref}/R_1$ .

### B. Design challenges of bandgap reference in wide operation temperature range

According to equation (1), the conventional bandgap reference can only compensate the linear part of the negative temperature coefficient of V<sub>BE</sub>. However, the temperature dependence of V<sub>BE</sub> has a nonlinear part [5]:

$$V_{BE}(T) = V_{BG} - (V_{BG} - V_{BE0}) \frac{T}{T_0} - (\eta - \alpha) V_T \ln \frac{T}{T_0} \quad (2)$$

where  $T$  is the absolute temperature;  $T_0$  is the reference temperature;  $V_{BG}$  is the bandgap voltage of silicon;  $\eta$  is a constant depending on doping level and it normally equals to 4;  $\alpha$  is a constant depending on the temperature character of the collector current in BJT. Therefore, the output reference cannot be purely temperature independent [5].

The PSRR of the circuit in fig. 1 can be written as:

$$PSRR = \frac{dV_{REF}}{dV_{dd}} = \frac{dV_{REF}}{dV_G} \cdot \frac{dV_G}{dV_{dd}} \quad (3)$$

where  $V_G$  is the voltage of the gate of MOS transistors.

Due to the feedback loop constitutes of the operational amplifier and the current mirror of  $M_1$  to  $M_4$ ,  $dV_G/dV_{dd}$  is inversely proportional to the loop gain of the feedback loop [6], or:

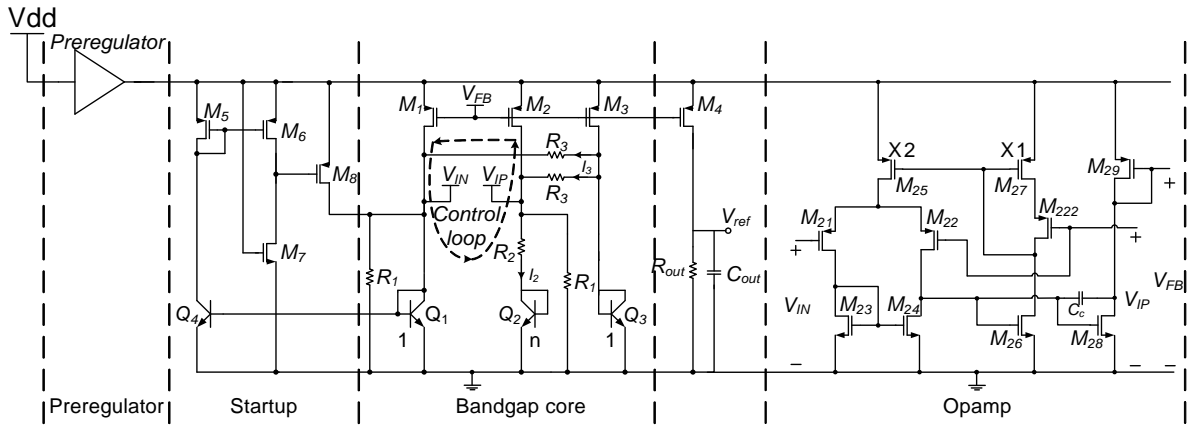


Fig. 2 The schematic of proposed bandgap reference.

$$\frac{dV_G}{dV_{dd}} = \frac{1}{1 + A_{vloop}} = \frac{1}{1 + A_v g_{m_{M2}} [R_1 // (R_2 + 1/g_{m_{Q2}})]} \quad (4)$$

where  $A_{vloop}$  is the loop gain of the control loop, and  $A_v$  is the gain of opamp. Here, the gain from  $V_{dd}$  to  $V_G$  without the feedback loop control is unity. Also, it can be derived that:

$$\frac{dV_{ref}}{dV_G} = g_{m_{M4}} R_{ref} \quad (5)$$

Combine (3) with (4) and (5), The PSRR of the circuit is:

$$PSRR = \frac{g_{m_{M4}} R_{ref}}{1 + A_v g_{m_{M2}} [R_1 // (R_2 + 1/g_{m_{Q2}})]} \quad (6)$$

Obviously, the PSRR of a bandgap is determined by the gain of the opamp. The gain of an opamp is constrained by its topology, power dissipation, and stability requirements. Consequently, it is difficult to improve the PSRR performance by simply enhancing the gain of the opamp under the circumstance of a bandgap reference, where power dissipation and chip area are of great importance. Some researches [7] [8] proposed extra circuits to gain a higher PSRR, but they needed either complex structures or precise element matching.

To guarantee that the circuit can work in a wide operation temperature range, some high order circuit nonidealities should be taken into account. For instance, the input offset of the opamp is a major error source in a reference circuit and it is also temperature dependent. A large opamp offset will degrade the temperature performance of the reference, especially in a wide operation temperature range [9]. Another example is the temperature coefficient of the power supply voltage. The temperature dependent variation of the power supply voltage will also increase the temperature coefficient of the reference.

### III. THE PROPOSED BANDGAP REFERENCE

To overcome the challenges mentioned above, a bandgap reference with curvature compensation, low offset opamp and a preregulator is proposed. The proposed bandgap reference is shown in fig. 2.

In fig.2, curvature compensation of  $V_{BE}$  as well as a low offset opamp is incorporated to achieve low temperature drift.

The input of the reference is regulated by a preregulator, which is temperature compensated, to improve power supply rejection.

#### A. Curvature compensation of $V_{BE}$

In Fig. 2, the topology of a current mode bandgap reference is adopted to form the first order compensation  $V_{BE}$  of BJT. The current on resistor  $R_2$  is

$$I_2 = \frac{V_{BE1} - V_{BE4}}{R_2} = \frac{V_T \ln n}{R_2} \quad (7)$$

Where  $n$  is the emitter area ratio. Consequently,  $I_2$  is proportional to absolute temperature (PTAT). As is mentioned in section 2.2,  $V_{BE}$  has a nonlinear portion with respect to temperature, so it is inadequate to compensate  $V_{BE}$  just by a PTAT voltage produced by  $I_2$ . Note that the collector current of Q1 is also PTAT due to the feedback, according to [8]:

$$V_{BE1}(T) = V_{BG} - (V_{BG} - V_{BE0}) \frac{T}{T_0} - (\eta - 1) V_T \ln \frac{T}{T_0} \quad (8)$$

From [8], if the collector current is independent of temperature, the  $V_{BE}$  can be written as:

$$V_{BE}(T) = V_{BG} - (V_{BG} - V_{BE0}) \frac{T}{T_0} - \eta V_T \ln \frac{T}{T_0} \quad (9)$$

Subtract (9) from (8), a nonlinear temperature-dependent voltage is obtained:

$$V_{NL} = V_T \ln \frac{T}{T_0} \quad (10)$$

In Fig.2,  $V_{NL}$  is equal to the difference of  $V_{BE1}$  and  $V_{BE6}$ , and a nonlinear current  $I_3$  is generated through  $R_3$ . Combine (7) to (10), the reference voltage of the proposed reference is

$$V_{ref} = \frac{R_{out}}{R_1} \left( V_{BE} + \frac{R_2}{R_1} V_T \ln n + \frac{R_3}{R_1} V_{NL} \right) \quad (11)$$

#### B. The preregulator

In fig.2, a preregulator is connected between the power supply and the reference circuit to reduce power supply dependence of the circuit, which is shown in fig.3. Through a

small-signal analysis, the PSRR of the entire circuit is given by [9]:

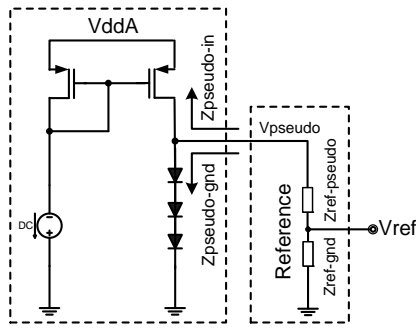


Fig. 3 The scheme of the preregulator.

$$PSRR = PSRR_{ref} \cdot PSRR_{pre} \quad (9)$$

where  $PSRR_{ref}$  and  $PSRR_{pre}$  are the PSRR of the reference circuit and the preregulator, respectively.  $PSRR_{ref}$  is obtained in section 2.2. A preregulator can be formed by incorporating the voltage drop on forward biased diodes [9] or by the method proposed in [11]. However, the voltage drop on forward diodes has a negative temperature drift of  $-2\text{mV}/^\circ\text{C}$ . And the performance of the circuit used in [11] is also jeopardized by the temperature drift of MOS threshold voltage, which is between  $-4\text{mV}/^\circ\text{C}$  and  $-2\text{mV}/^\circ\text{C}$ .

These temperature drifts have noticeable influence on the reference temperature coefficient, especially in the situation where the operation temperature range is wide, because the PSRR of reference will degrade dramatically under extreme high temperatures ( $125^\circ\text{C}$ ). Consequently, temperature compensation is employed in preregulator in this paper. The proposed preregulator is shown in fig.4.

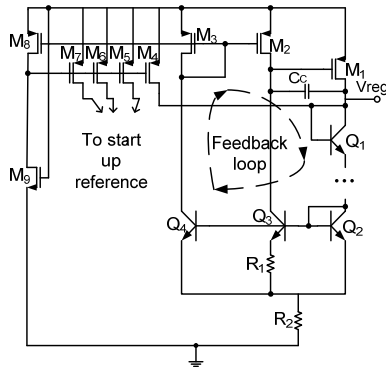


Fig. 4 Proposed preregulator.

It can be verified that the output of the preregulator is:

$$V_{reg} = mV_{BE} + \frac{R_5}{R_4} V_T \ln n \quad (10)$$

where  $n$  is the emitter area ratio of BJT  $Q_9$  to  $Q_{10}$ , and  $m$  is the number of cascading BJTs. With a carefully setting of  $R_5$  and  $R_4$ , the output voltage of the preregulator can be first order temperature independent.

As it is derived in [6], the PSRR of the preregulator is inversely proportional to the loop gain which is used the feedback loop. To calculate the loop gain, first consider the gain from the gate of  $M_1$  to  $V_{reg}$ :

$$A_{v1} = gm_{M1} [r_{oM1} // (\frac{1}{gm_{Q2}} + \frac{1}{gm_{Q1}} + R_2)] \quad (11)$$

Secondly, consider the gain from the base of  $Q_4$  to the gate of  $M_2$ :

$$A_{v2} = \frac{gm_{Q4}}{1 + gm_{Q4}R_2} \frac{1}{gm_{M3}} \approx \frac{1}{R_2 gm_{M3}} \quad (12)$$

Finally, consider the gain from the gate of  $M_2$  to  $M_1$ :

$$A_{v3} = gm_{M2} \{r_{oM2} // [r_{oQ3} gm_{Q3} (R_1 + R_2)]\} \quad (13)$$

Combine the equation (11) to equations (12) and (13) while notice that  $gm_{Q1}=gm_{Q2}=gm_{Q3}=gm_{Q4}$  and  $gm_{M1}=gm_{M2}=gm_{M3}$ , the PSRR of preregulator can be written as:

$$PSRR_{pre} = \left\{ \frac{r_{oM1} + 2/gm_{Q1} + R_2}{2/gm_{Q1} + R_2} \cdot \frac{gm_{M1}}{R_2} [r_{oM1} // (\frac{2}{gm_{Q1}} + R_2)] \cdot \left\{ r_{oM2} // [r_{oQ3} gm_{Q3} (R_1 + R_2)] \right\} \right\}^{-1} \quad (14)$$

In equation (14), the first term is the gain from power supply to  $V_{reg}$  without the effect of the feedback loop control, and the last two terms represent the loop gain of the feedback loop. Using equations (6), (9) and (14), the PSRR of the reference is determined by the product of the gain of the two control loops used in the bandgap circuit and preregulator. As a result, the PSRR of the reference can be improved by more than 60dB.

The output voltage is controlled by the number of the cascaded BJTs, and can be written as:

$$V_{out} = m \cdot V_{BG} \quad (15)$$

where  $m$  is the number of the cascaded BJTs and  $V_{BG}$  is the bandgap voltage of silicon. Equation (15) indicates that the minimum value of power supply voltage of the reference is  $V_{BG} + V_{ds}$ , which is about 1.5V.

### C. The design of opamp

Fig. 2 also shows the schematic of the opamp. To guarantee that the input offset will not increase the temperature coefficient, a low offset opamp structure is used[12]. Instead of NMOS in [12], two PMOS transistors are used as the input pair since PMOS transistors have lower flick noise. The MOS Transistors  $M_{21}$ ,  $M_{22}$ ,  $M_{23}$ ,  $M_{24}$  form an input differential pair and a current-mirror load. Global feedback in fig. 2 sets  $V_{FB}$ , which is the voltage from the opamp output to ground and is used to control the drain current of the current mirror in bandgap circuit. The drain current of  $M_{26}$  is fed back to the gate of transistor  $M_{27}$  and  $M_{25}$  to self bias the opamp. In order to eliminate the systematic offset of the self-biased feed back loop, a replica transistor of  $M_{22}$  is used to equalize the source-drain voltage of  $M_{25}$  and  $M_{27}$ .

The gain of the opamp is:

$$A_v = Gm_{21} \cdot (R_{dsN} // R_{dsP}) \cdot \frac{Gm_{28}}{Gm_{29}} \quad (16)$$

where  $R_{dsN}$  and  $R_{dsP}$  are the output resistance of NMOS and PMOS, respectively. A proper design of the aspect ratio of M28 and M29 can achieve a gain of the opamp as high as 60dB; this could minimize the gain error.  $C_c$  provides the Miller compensation to ensure the stability.

The minimum power supply can be calculated by:

$$V_{dd} = V_{BE} + V_{thp} + V_{ds} \quad (17)$$

From (17), the minimum supply voltage to the opamp is around 2V. If lower power supply is critical in designing the circuit, the opamp circuit of [10] can be used for a lower voltage operation while sacrificing the noise performance. The circuit's stimulation features are summarized in table 1:

Tab. 1 Performance summary of the proposed opamp.

DC gain	66 dB
Bandwidth	3.4 MHz
Phase margin	70°
Offset voltage	100μV
Output range	200mV-2V

#### D. Noise attenuation

Because that output voltage of the reference is a DC voltage, both wide band “white” noise and narrow band “flicker” noise are critical to the final performance. As for wide band white noise, reducing the bandwidth of the output voltage is a clear choice. Consequently, a bypass capacitor,  $C_{out}$ , is connected to the output of the reference to filter out high frequency noise.

Flick noise, on the other hand, can be express as:

$$\bar{I}_n^2 = \frac{K}{C_{ox}WL} \cdot \frac{1}{f} \cdot Gm^2 \quad (18)$$

where  $K$  is a constant and is determined by process parameters. From (18) it can be concluded that flick noise can be reduced by larger the transistor area and lower the transconductance. Thus, when designing the current mirror of Fig.2, long PMOS transistors with small aspect ratio are used both for reducing flicker noise and reducing the channel length modulation, which can introduce offset to the reference circuit.

#### E. Startup circuit

To prevent the bandgap circuit from working on the “dead” point where there are no current in all branches of the circuit, a startup circuit formed by M5-M8 is shown in Fig.2. When the circuit works on the “dead” point, the voltage at gate of M5 is approaching  $V_{dd}$ , which, through the inverter composed of M6 and M7, will turn M8 on and start the bandgap circuit on. And when the circuit is working on the normal point, the gate voltage of M8 will be pulled high and therefore turn off M8.

## IV. SIMULATION AND TEST RESULTS

The circuit is simulated with Cadence Spectre®, based on the BSIM v3.3 model. Table 2 summaries the simulation results of the circuit:

Tab. 2 Simulation of the proposed bandgap circuit.

Supply Voltage	3V
Total Power	405.1μW
RMS Noise	3.35μV
TC	0.68ppm/°C
PSRR	135dB@DC
Liner Regulation	142.36nV/V
Voltage at 27°C	939.045 mV

In table 2, the TC is calculated using the following equation:

$$TC = (V_{\max} - V_{\min}) / (V_{\text{normal}} \cdot 180) \quad (18)$$

where  $V_{\text{normal}}$  is the voltage at 27°C, and “180” is the full temperature range.

The circuit is a part of a pipelined ADC and the micrograph is shown in fig.4. It occupies an area of  $550 \times 300 \mu\text{m}^2$ . The chip was taped out in a  $0.5 \mu\text{m}$  BiCMOS technology. To test its power dissipation, the reference has an independent power supply.

In Fig.5, the upper graph is the obtained reference voltage against the variation of the temperature. It can be seen that although the temperature range is wide (from -55°C to 125°C), the temperature coefficient of the reference is 5.8ppm/°C, at the same level with that reported in [11]. The lower graph shows the PSRR of the reference under 3 different temperatures: -55°C, 27°C and 125°C. It can be seen that PSRR is 92dB at DC. A 1μF off chip bypass capacitor helps to increase the PSRR when the frequency is higher than 100 kHz.

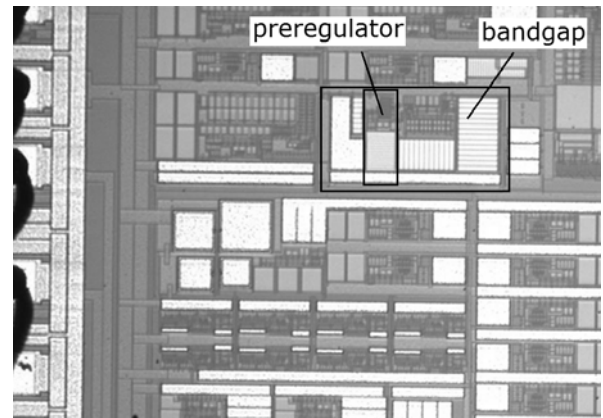


Fig.5. The micrograph of the reference circuit

Fig. 6(a) and Fig. 6(b) demonstrates the tested result of the reference circuit. Table 3 summarizes the performance of the reference and compares it with other reported bandgap references. From table 3, it can be shown that in paper [11], the temperature coefficient is low (7ppm/°C), and the PSRR is high. However, the circuit can only work in a relative narrow temperature range (-20°C ~80°C) and consume more

power (3mW). As for the work in [12], the temperature coefficient high (10 ppm/°C) and the PSRR is low (68dB). In this work, the reference achieves a low temperature coefficient of 5.8 ppm/°C, a wide operating temperature range over -55°C to 125°C and a high PSRR of 92dB. Besides, the reference's power dissipation is reasonable (462μW).

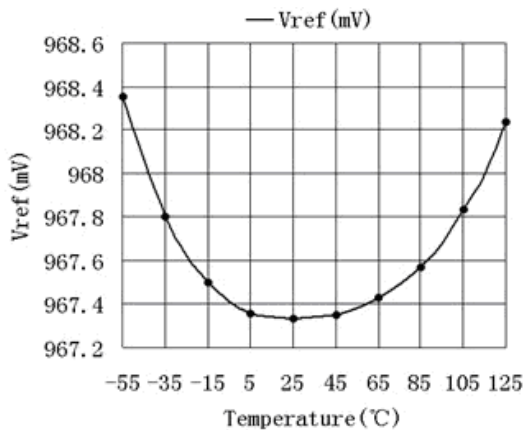


Fig. 6(a): Vref VS temperature

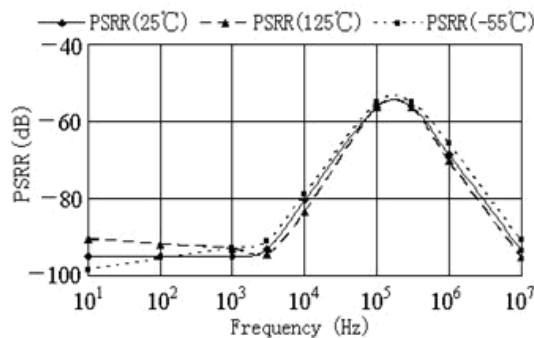


Fig. 6(b): The PSRR of the bandgap circuit

Tab. 3 Performance comparison of this work to resent studies.

Parameters	This work	[11].2005	[12] 2007
Technology	0.5μm BiCMOS	0.8μm BiCMOS	0.35μm CMOS
Vdd	3V	3V	1.4V
Power dissipation	462μW	3mW	162μW
Temperature Range	-55°C ~125°C	-20°C ~80°C	-20°C ~120°C
TC	5.8 ppm/°C	7ppm /°C	10 ppm/°C
Reference voltage at 27°C	967 mV	1.45V	858mV
PSRR at DC	92dB	94dB	68dB

## V. CONCLUSION

A curvature compensated bandgap reference with a wide operation temperature range is designed in 0.5μm BiCMOS technology in this paper. The reference is based on the current mode bandgap configuration. Accurate compensation of the output voltage temperature dependence is obtained with a simple but very effective implementation of the curvature correction technique. A preregulator with low temperature drift is designed, and a self-biased opamp with reduced offset is introduced. The whole circuit has a power dissipation of 462μW under the power supply voltage of 3V. The output voltage has a temperature coefficient of 5.8ppm/°C over the temperature range of -55°C to 125°C. The PSRR of the reference at DC is 92dB. Besides, a 1μF off chip bypass capacitor increase the PSRR when frequency is higher than 100 kHz.

## REFERENCES

- [1] AD7738 data sheet <http://www.analog.com>
- [2] ADS1282 data sheet <http://www.ti.com>
- [3] Karel E.Kuijk, "A precision reference voltage source", IEEE Journal of Solid-State Circuits, vol.sc-8, No. 3, June 1973.
- [4] Brokaw, P., "A simple three-terminal IC bandgap reference", IEEE Journal of Solid-State Circuits, vol. 9, pp. 388-393, Dec 1974.
- [5] R. Mora, Voltage references: from diodes to precision high-order bandgap circuits, New York: John Wiley & Sons, 2002.
- [6] Steyaert, M.S.J. and Sansen, W.M.C., "Power Supply Rejection Ratio in Operational Transconductance Amplifiers" Circuits and Systems, IEEE Transactions on, vol. 37 no. 9, pp. 1077-1084, Sep 1990.
- [7] Low voltage bandgap circuit with improved power supply ripple rejection, C. Jun and H. S. Kuok, US patent 6507179.
- [8] High PSRR, high accuracy, low power supply bandgap circuit, D. L. Zupcau and S. Meyers US patent 7199646.
- [9] Behzad Razavi. Design of Analog CMOS Integrated Circuits. Beijing: Tsinghua University Press, 2005.
- [10] Piero Malcovati, et al., "Curvature-Compensated BiCMOS Bandgap with 1-V Supply Voltage", IEEE J. Solid-State Circuits, Vol. 36, No. 7, JULY 2001, pp. 1076-1081.
- [11] Xiao Du, Li Wei-min, Zhu Xiao-fei, Fu Xiao-dong "A curvature-compensated bandgap reference with improved PSRR" ASIC, 2005, Vol.2, pp. 529-533
- [12] Raymond T. Perry, Stephen H. Lewis, A. Paul Brokaw, and T. R. Viswanathan "1.4 V Supply CMOS Fractional Bandgap Reference", IEEE Journal of Solid-State Circuits, Vol. 42, No. 10, OCTOBER 2007, pp. 2180-2186.